Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (previously amended) A system interface comprising:

(a) a plurality of first director boards, each one of the first director boards having:

(i) a plurality of first directors; and

(ii) a crossbar switch having input/output ports coupled to the first directors on such one of the first director boards and a pair of output/input ports;

(b) a plurality of second director boards, each one of the second directors boards having:

(i) a plurality of second directors; and

(ii) a crossbar switch having input/output ports coupled to the second directors on such one of the second director boards and a pair of output/input ports;

(c) a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors;

(d) a message network, operative independently of the data transfer section, coupled to the pair of output/input ports of each one of the directors boards of the plurality of first director boards and to the pair of output/input ports of each one of the directors boards of the plurality of second director boards; and

(e) wherein the first and second directors control data transfer between the first directors and the second directors in response to messages passing between the first directors and the second directors through the message network to facilitate data transfer between first directors and the second directors with such data passing through the cache memory in the data transfer section.

2. (original) The system interface recited in claim 1 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a controller for transferring the messages between the message network and such one of the first directors.

3. (original) The system interface recited in claim 1 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

4. (original) The system interface recited in claim 2 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

5. (original) The system interface recited in claim 1 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the first directors and

for controlling the data between the input of such one of the first directors and the cache memory.

6. (original) The system interface recited in claim 1 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

7. (original) The system interface recited in claim 5 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

8. (previously amended) A data storage system for transferring data between a host computer/server and a bank of disk drives through a system interface, such system interface comprising:

(a) a plurality of first director boards coupled to host computer/server; each one of the first director boards having:

(i) a plurality of first directors; and

(ii) a crossbar switch having input/output ports coupled to the first directors on such one of the first director boards and a pair of output/input ports;

(b) a plurality of second director boards coupled to the bank of disk drives, each one of the second director boards having:

(i) a plurality of second directors; and

(ii) a crossbar switch having input/output ports coupled to the second directors on such one of the second director boards and a pair of output/input ports;

(c) a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors;

(d) a message network, operative independently of the data transfer section, coupled to the pair of output/input ports of each one of the directors boards of the plurality of first director boards and to the pair of output/input ports of each one of the directors boards of the plurality of second director boards; and

(e) wherein the first and second directors control data transfer between the host computer and the bank of disk drives in response to messages passing between the first directors and the second directors through the message network to facilitate the data transfer between host computer/server and the bank of disk drives with such data passing through the cache memory in the data transfer section.

9. (original) The system interface recited in claim 8 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a controller for transferring the messages between the message network and such one of the first directors.

10. (original) The system interface recited in claim 8 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

11. (original) The system interface recited in claim 9 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

12. (original) The system interface recited in claim 8 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the first directors and for controlling the data between the input of such one of the first directors and the cache memory.

13. (original) The system interface recited in claim 8 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

14. (original) The system interface recited in claim 12 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

15. (previously presented) A system interface comprising:

(a) a plurality of first director boards, each one of the first director boards having:

(i) a plurality of first directors; and

(ii) a crossbar switch having input/output ports coupled to the first directors on such one of the first director boards and an output/input port;

(b) a plurality of second director boards, each one of the second directors boards having:

(i) a plurality of second directors; and

(ii) a crossbar switch having input/output ports coupled to the second directors on such one of the second director boards and an output/input port;

(c) a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors;

(d) wherein the data transfer section is also coupled to the output/input port of the crossbar switch of each one of the plurality of first director boards and to the output/input port of the crossbar switch of each one of the plurality of second director boards;

(e) a message network, operative independently of the data transfer section; and

(e) wherein the first and second directors control data transfer between the first directors and the second directors in response to messages passing between the first directors and the second directors through the message network to facilitate data transfer between first directors and the second directors with such data passing through the cache memory in the data transfer section.

16. (previously presented) The system interface recited in claim 15 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a controller for transferring the messages between the message network and such one of the first directors.

17. (previously presented) The system interface recited in claim 15 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

18. (previously presented) The system interface recited in claim 16 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

19. (previously presented) The system interface recited in claim 15 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the first directors and for controlling the data between the input of such one of the first directors and the cache memory.

20. (previously presented) The system interface recited in claim 15 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

21. (previously presented) The system interface recited in claim 19 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

22. (previously presented) A data storage system for transferring data between a host computer/server and a bank of disk drives through a system interface, such system interface comprising:

(a) a plurality of first director boards coupled to host computer/server; each one of the first director boards having:

(i) a plurality of first directors; and

(ii) a crossbar switch having input/output ports coupled to the first directors on such one of the first director boards and an output/input port;

(b) a plurality of second director boards coupled to the bank of disk drives, each one of the second director boards having:

(i) a plurality of second directors; and

(ii) a crossbar switch having input/output ports coupled to the second directors on such one of the second director boards and an output/input port;

(c) a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors;

(d) wherein the data transfer section is also coupled to the output/input port of the crossbar switch of each one of the plurality of first director boards and to the output/input port of the crossbar switch of each one of the plurality of second director boards;

(e) a message network, operative independently of the data transfer section; and

(f) wherein the first and second directors control data transfer between the host computer and the bank of disk drives in response to messages passing between the first directors and the second directors through the message network to facilitate the data transfer between host computer/server and the bank of disk drives with such data passing through the cache memory in the data transfer section.

23. (previously presented) The system interface recited in claim 22 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a controller for transferring the messages between the message network and such one of the first directors.

24. (previously presented) The system interface recited in claim 22 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

25. (previously presented) The system interface recited in claim 23 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

26. (previously presented) The system interface recited in claim 22 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the first directors and for controlling the data between the input of such one of the first directors and the cache memory.

27. (previously presented) The system interface recited in claim 22 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

28. (previously presented) The system interface recited in claim 26 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors

and for controlling the data between the input of such one of the second directors and the cache memory.

29. (previously presented) A system interface comprising:

(a) a plurality of first director boards, each one of the first director boards having:

(i) a plurality of first directors; and

(ii) a crossbar switch having input/output ports coupled to the first directors on such one of the first director boards and an output/input port;

(b) a plurality of second director boards, each one of the second directors boards having:

(i) a plurality of second directors; and

(ii) a crossbar switch having input/output ports coupled to the second directors on such one of the second director boards and an output/input port;

(f) a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors;

(g) wherein the data transfer section is also coupled to the output/input port of the crossbar switch of each one of the plurality of first director boards and to the output/input port of the crossbar switch of each one of the plurality of second director boards;

(h) a message network, operative independently of the data transfer section; and

(f) wherein the first and second directors control data transfer between the first directors and the second directors in response to messages passing between the first directors and the second directors through the messaging network with such messages by-passing the data transfer section and with such data transfer comprising passing data through the directors to the cache memory in the data transfer section.

30. (previously presented) A system interface comprising:

(a) a plurality of first director boards, each one of the first director boards having:

(i) a plurality of first directors, each one of the directors having a data port and a message port; and

(ii) a crossbar switch having input/output ports coupled to the message ports of the first directors on such one of the first director boards and a pair of output/input ports;

(b) a plurality of second director boards, each one of the second directors boards having:

(i) a plurality of second directors, each one of the directors having a data port and a message port; and

(ii) a crossbar switch having input/output ports coupled to the message ports of the second directors on such one of the second director boards and a pair of output/input ports;

(c) a data transfer section having a cache memory, such cache memory being coupled to the data ports of the plurality of first and second directors;

(d) a message network, coupled to the pair of output/input ports of each one of the directors boards of the plurality of first director boards and to the pair of output/input ports of each one of the directors boards of the plurality of second director boards; and

(e) wherein the first and second directors control data transfer between first director and the second director with data in such data transfer passing through the cache memory in response to messages passing between the first director and the second director through the messaging network.

31. (previously presented) A system interface comprising:

(a) a plurality of first director boards, each one of the first director boards having:

(i) a plurality of first directors; and

(ii) a crossbar switch having input/output ports coupled to the first directors on such one of the first director boards and a pair of output/input ports;

(b) a plurality of second director boards, each one of the second directors boards having:

(i) a plurality of second directors; and

(ii) a crossbar switch having input/output ports coupled to the second directors on such one of the second director boards and a pair of output/input ports;

(c) a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors;

(d) a message network, operative independently of the data transfer section, coupled to the pair of output/input ports of each one of the directors boards of the plurality of first director boards and to the pair of output/input ports of each one of the directors boards of the plurality of second director boards;

(e) wherein the first and second directors control data transfer between first director and the second director with data in such data transfer passing through the cache memory in response to messages passing between the first director and the second director through the messaging network; and

(f) wherein each one of the messages includes a destination field.